

## Effect of the Geometry of Slots and Splits on EMI Level of PCBs: A Parametric Study

Seyit Ahmet Sis<sup>(1),(2)</sup>, and Fatih Üstüner\*<sup>(1),(3)</sup>

(1) TUBITAK BILGEM, Gebze, Kocaeli, Turkey

(2) Balıkesir University, Balıkesir, Turkey

(3) Istanbul Commerce University, İstanbul, Turkey

### Abstract

A defect on the reference plane, when crossed over by a signal trace on the signal line, is a primary source for unwanted electromagnetic radiation in printed circuit boards (PCBs). Such a defect either completely cleaves the reference plane into two pieces by means of forming a split between them or partially divides the reference plane by means of forming a slot with a short on at least one end of the defect. This paper presents a detailed parametric study on these defects focusing on how electromagnetic interference (EMI) level varies as a function of geometric parameters. In this regard, first, the width of a slot and a split is systematically varied, and electric field at 3 m away from the PCB is simulated, by keeping the lengths of the slot and split constant. Then, the same simulations are repeated by keeping the width constant and varying the length of the defect. Simulation results show that the length of the defect is an ultimate determinative parameter in the radiation characteristics of the defect. The measurement results for two PCBs; one with a slot and another with a split on the ground plane are also presented.

### 1 Introduction

In complex PCBs, multiple DC potentials, serving as either different bias voltages or ground levels, exist in a single board. These multiple voltage levels are realized as power and ground islands on the reference planes [1]-[2], forming split-type defects between the islands. The reference planes are sometimes partially separated such that at least one end of the defect is short circuit loaded, creating a slot-type defect. These slots are mostly utilized in mixed-signal circuits when digital and analog circuits share a common DC ground level [3]. They exhibit high impedance on the return current path to isolate the sensitive analog/RF circuit from the noisy digital circuit [3]-[5].

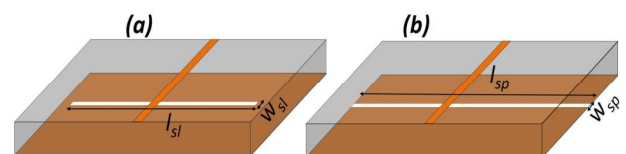
A signal trace passing over a split or slot between two power or ground islands results in a discontinuity on the return current path. The current, in fact, is forced to make a round trip around the slot, and/or flows as a displacement current over the capacitance on the slot. This elongated return current path act as a decent radiator and causes EMI issues [6]-[9]. A common approach is to employ a so-called stitching capacitor over the defect to selectively reduce the impedance on the return current path, hence limit the EMI [10]-[14]. Another approach is to engineer the shape of the

defect to reduce the radiation [15]-[18]. Tapered, corrugated, trident incurvature, and interdigital (meandered shape) defected ground structures are reported.

In this paper, a detailed parametric study on the slot and splits are performed, focusing on how electromagnetic interference (EMI) level varies as a function of geometric parameters. In this regard, first, the width of a slot and a split is systematically varied, and electric field at 3 m away from the PCB is simulated, by keeping the lengths of the slot and split constant. Then, the same simulations are repeated by keeping the width constant and varying the length of the defect. Simulation results show that the length of the defect is an ultimate determinative parameter in the radiation characteristics of the defect.

### 2 The Structure and EM Simulations

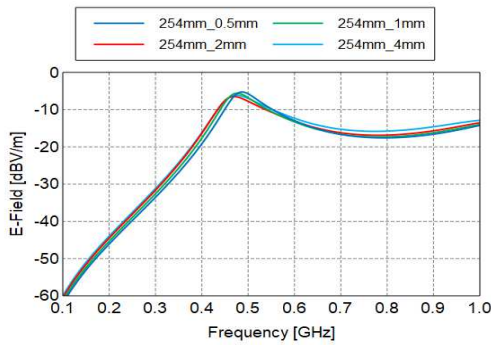
The basic structure consists of a rectangular PCB. The length and the width of the PCB are 300 mm and 200 mm respectively. On the top layer of the PCB, there is a microstrip line crossing through the width of the PCB. On the bottom side of the PCB, there is a ground plane on which a slot is placed orthogonal to the top layer microstrip line while keeping symmetry with respect to it. This slot is lengthened until a complete split is obtained throughout the ground plane. A microstrip line crossing over a slot on the reference plane is shown in Fig. 1 (a). The same structure with a split on the reference plane is shown in Fig. 1 (b).



**Figure 1.** The structure for (a) a slot on the ground plane crossed by a microstrip line, and (b) a split on the ground plane crossed by a microstrip line.

The length and width of the slot are represented by  $l_{sl}$  and  $W_{sl}$ , respectively, as shown in Fig. 1 (a). Similarly, the length and width of the split are represented by  $l_{sp}$  and  $W_{sp}$ , respectively. The length of the microstrip line is 200 mm. The width of the microstrip line is 2.3 mm, providing a characteristic impedance of approximately  $50 \Omega$  ( $Z_0 = 50 \Omega$ ). The PCB is made of a FR4 dielectric layer with a thickness of 1.55 mm and a dielectric constant of 4.6 ( $\epsilon_r = 4.6$ ).

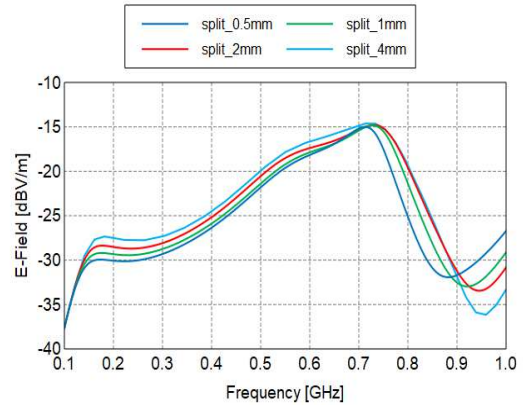
Three different parametric studies are performed. In the first parametric study (configuration #1), the slot length is kept at 254 mm while changing the width of the slot from 0.5 mm to 4 mm by doubling the width at each step (namely 0.5 mm, 1 mm, 2 mm, and 4 mm). In the second parametric study (configuration #2), the slot is lengthened to 300 mm until a complete split is obtained. In this configuration also, the width of the split is the parameter that is changed from 0.5 mm to 4 mm by doubling the step size. In the final parametric study (configuration #3), the width of the slot is kept constant at 0.5 mm while changing the slot length from a complete split (300 mm) to 50 mm by decreasing the length with a 50 mm step size (since 254 mm length analysis is available it replaced the 250 mm analysis). The structures are modeled using the computational electromagnetics tool FEKO. The microstrip line is fed by 1 V with a 50 ohm source impedance and is terminated with 50 ohm load. The method of moments extended with the volume equivalence principle (VEP) is chosen as the solver. The analysis is carried out between 100 MHz and 1 GHz. The total electric field obtained at 3 meters away from the PCB board is presented for the three cases in Figures 2, 3, and 4.



**Figure 2.** Simulated E-field for different slot widths ( $W_{sl}=0.5\text{mm}, 1\text{mm}, 2\text{mm}, 4\text{mm}$ ) when  $l_{sl}=254$  mm.

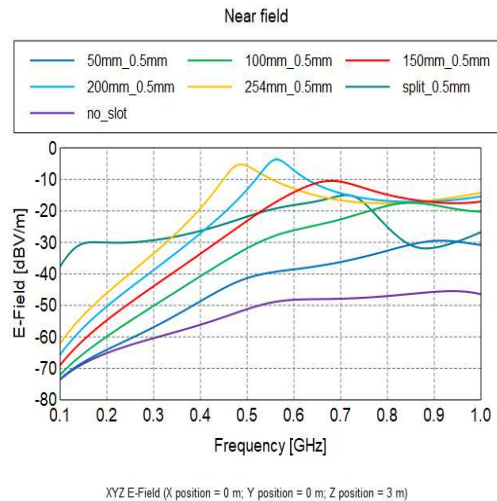
In configuration #1, in all cases, the radiated electric field starts increasing until making a peak around 450 MHz, and then it leveled off around -15 dBuV/m (Fig. 2). There occurs a slight difference in magnitude between the radiated fields as the slot width changes. It can be said that changing the slot width does not change the radiated emission significantly. As seen in Fig.2, in configuration #2, the radiated electric field, again in all configurations, starts increasing and reaches a maximum level of -15 dBuV/m between 650 MHz and 750 MHz. Then it decreases to -30 dBuV/m towards 900 MHz and then starts to increase again (Fig. 3). The changing the split width pronounces more in this case but the results still do not differ much from each other. Unlike configurations #1 and #2, configuration #3 illustrates dramatic changes in the radiated electric field by changing the length of the slot. As seen in Fig. 4, to understand the emission characteristics, it is better to go from the no-slot case to the full split case. The no-slot case which can be considered as a reference case gives minimum radiated emission as expected. When a slot is of length 50 mm, the structure begins to radiate as much as 10 to 15 dB increasing as one goes to higher frequencies. Then, if we increase the slot length to 100 mm,

the emission level increases around 10 dB. With a further 50 mm increase in slot length (150 mm case), the emission increases by 10 dB again at middle frequencies.



**Figure 3.** Simulated E-field for different split widths ( $W_{sl}=0.5\text{mm}, 1\text{mm}, 2\text{mm}, 4\text{mm}$ ) when  $l_{sp}=300$  mm

In case 150 mm slot length, we notice that a moderate peak begins to form around 680 MHz. When we increase the slot length to 200 mm, the emission is larger until 600 MHz, after then exhibits a similar emission profile like the 150 mm case. Moreover, the peak which occurs this time at 560 MHz, exhibited itself more strongly. The same thing can be said for the 254 mm slot length case except for the fact that its peak is shifted to 480 MHz. The formation of a peak and its shifting to lower frequencies as the slot length increases implies that the slot behaves like a printed slot antenna.



**Figure 4.** Simulated E-field for different slot lengths ( $l_{sl}=0.5\text{mm}, 1\text{mm}, 2\text{mm}, 4\text{mm}$ ) when  $W_{sp}=0.5$  mm

The physical difference between the printed slot antenna and the analyzed structure is that the latter's excitation microstrip line is not left open. It is terminated with its characteristic impedance. The split case emission profile completely differs from the slot cases. It begins to radiate at much lower frequencies but do not show a sharp peak and exhibits a broadband nature. It can be said that as the length of the slot increases, the level of radiated emissions and the split case exhibits broadband radiated emission characteristics.

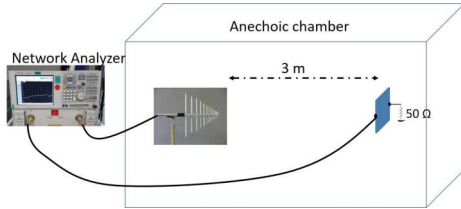
### 3 Measurement Results

Two circuits: one with a microstrip line crossing a slot on the ground plane and another one crossing a split on the ground plane are fabricated on an FR4 substrate. The geometric parameters of the fabricated circuits are given in Table I.

**Table I.** Geometric Parameters of the Fabricated PCBs

	<i>Circuit with slot</i>	<i>Circuit with split</i>
$W_{sl}$	0.5 mm	---
$l_{sl}$	254 mm	---
$W_{sp}$	---	0.5 mm
$l_{sp}$	---	300 mm
<i>Microstrip length</i>	200 mm	200 mm
<i>Microstrip width</i>	2.3 mm	2.3 mm

A reference circuit with no slot/split is also fabricated for comparison purposes. EMI levels from both PCBs are measured in an anechoic chamber 3 m away from the PCB. The measurement setup and a photograph during measurement are shown in Fig. 5 and Fig. 6, respectively. In the radiation emission measurement setup, the first port of the network analyzer is connected to one of the ports of the PCB board. The second port of the network analyzer is connected to a Schwarzbeck UHALP 9108A1 log-periodic antenna. The other port of the PCB board is connected to a wideband 50  $\Omega$  load.



**Figure 5.** EMI measurement setup block diagram.

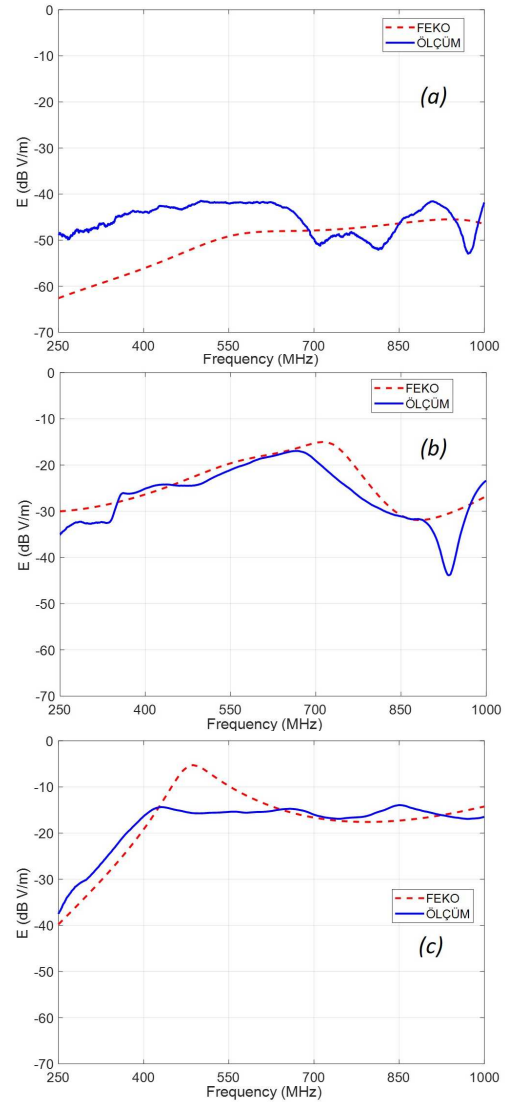


**Figure 6.** A photograph inside an anechoic chamber during measurements

The power level of the network analyzer is set to 0 dBm. The frequency range is set to 250 MHz -1 GHz range, and the system is calibrated via a short-open-load-thru (SOLT) calibration kit. Both the antenna and the PCB board are placed 1.5 m above the floor. The electric field is extracted from the measured  $S_{21}$  parameter as follows:

$$E(\text{dBV/m}) = 0 \text{ dBm} + S_{21} \text{ dB} + AF + 107 \text{ dB} - 120 \text{ dB} \quad (1)$$

where  $AF$  is the antenna factor. In (5), 107 dB is added to convert power level in dBm to voltage level in dB  $\mu$ V and -120 dB is added to convert dB  $\mu$ V to dB V. To verify the validity of simulation-based parametric analysis presented in the previous section, measurement results for the fabricated circuits are plotted as a function of frequency by comparing the with the simulation results. In general, simulation results show good agreement with the measurement results. Simulation results, for the circuit with a slot on the ground plane, exhibit a sharp peak at 480 MHz, which is not the case in measurement results.



**Figure 7.** Comparison of simulation and measurement results for the circuits (a) with no defect, (b) with a split, and (c) with a slot on the ground plane.

### 6 Conclusion

A parametric analysis is performed for rectangular slot- and split-type defects commonly available on reference planes. EMI level is systematically simulated as a function of these parameters and results are presented. A major

conclusion is that the length of the defect is the major parameter determining the radiation level. The width of the defect is not effective on the EMI level.

## 7 References

1. M. Mondal and B. Archambeault, "On inductance of power islands and its impact on decoupling behavior in high speed boards," 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Washington, DC, 2017, pp. 579–584, DOI:10.1109/ISEMC.2017.8077935.
2. B. R. Archambeault, and J. Drewniak, "Decoupling Power/Ground Planes in PCB Design for Real-World EMI Control", The Springer International Series in Engineering and Computer Science, vol. 696, 2002, DOI : 10.1007/978-1-4757-3640-3.
3. K. Jung, J. Lee, Y. Chung, and J. Choi, "Circuit model analysis for traces that cross a DGS," Journal of Electromagnetic Engineering and Science, vol.12, no. 4, pp. 240-246, Dec. 2012, DOI:105515/JKIEES.2012.12.4.240.
4. L. Shi, Z. Wei, and C. Wang, "EBG combined isolation slots with a bridge on the ground for noise suppression," International Journal of Electronics, vol. 103, pp.1726-1735, Jan.2016, DOI : 10.1080/00207217.2016.1138526
5. M. Kazerooni, A. Cheldavi, and M. Kamarei, "Crosstalk and electromagnetic interference noise investigation for a coupled pair of microstrip lines with a break in ground structure." IET Microwaves, Antennas & Propagation, vol.4, no.9, pp.1336-1346, Sep. 2010 , DOI:10.1049/IETMAP.2009.0180.
6. B. Archambeault, C. Brench and S. Connor, "Review of PrintedCircuitBoard Level EMI/EMC Issues and Tools," IEEE Transactions on Electromagnetic Compatibility, vol. 52, no. 2, pp. 455-461, May 2010, DOI: 10.1109/ TEMC.2010.2044182.
7. J. Kim, H. Lee, and J. Kim. "Effects on signal integrity and radiated emission by split reference plane on high-speed multilayer printed circuit boards," IEEE Transactions on Advanced Packaging, vol.28, no.4, pp.724735, Nov. 2005. DOI: 10.1109/TADVP.2005.850503.
8. T. E. Moran, K. L. Virga, G. Aguirre, and J. L. Prince, "Methods to reduce radiation from split ground planes in RF and mixed signal packaging structures," IEEE Transactions on Advanced Packaging, vol.25, no.3, pp.409-416, Aug. 2002, DOI: 10.1109/TADVP.2002.805997.
9. B. Archambeault, "Proper design of intentional splits in the ground reference plane of PC boards to minimize emissions on I/O wires and cables," 1998 IEEE EMC Symposium. International Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No.98CH36253), Denver, CO, USA, 1998, vol.2, pp. 768 – 773.
10. J. Roden, B. Archambeault, and R. Lyle, "Effect of stitching capacitor distance for critical traces crossing split reference planes," IEEE Symposium on Electromagnetic Compatibility, Symposium Record (Cat. No.03CH37446), Boston, MA, USA, vol.2, pp.703-707, 2003 , DOI: 10.1109/ISEMC.2003.1236692.
11. J. Lee, P. Lee, T. Lee, C. Kim, I. Song, and J. Wee, "Effect of split power/ground planes using stitching capacitors on radiated emission." 2009 11th Electronics Packaging Technology Conference.
12. Y. Ho, H. Hsu, J. Liao, and X. Cai, "Stitching impedance analysis of LPDDR power plane split and its impact to radio frequency interference (RFI) and signal integrity (SI)." 2017 IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS). San Jose, CA, USA, pp. 1 – 3, 2017, DOI: 10.1109/EPEPS.2017.8329745.
13. Z. Wen and Q. Wu, "Revisit of signal traces crossing split ground plane using characteristic mode analysis," 2017 Sixth Asia-Pacific Conference on Antennas and Propagation (A P C A P) , Xi'an, China, 2017, pp. 1 – 3, DOI: 10.1109/APCAP.2017.8420520.
14. S. A. Sis, E. Demirel, M.T. Mersin, F. Üstüner, "Baskı Devrelerde Donus, Yolu Uzerindeki Sureksizliklerden Kaynaklanan Elektromanyetik Girisinin Numerik Analizi ve Deneysel Dogrulanması" EMO Bilimsel Dergi, early access.
15. K. J. Bois, and B. Toby, "Defected ground structure to minimize EMI radiation," U.S. Patent 10 178 761, Jan. 8, 2019.
16. K. J. Bois, E. Chobanyan, and B. Toby, "Defected ground structure with void having resistive material along perimeter to improve EMI suppression." U.S. Patent 10 499 489, Dec. 3, 2019.
17. C. Kao, C. Chiu, Y. Chuang, T. Lin and H. Hsieh, "An effective EMI-suppression technique for modern wideband common-mode filters," 2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC), Singapore, 2018, pp. 986-990, DOI: 10.1109/ISEMC.2018.8393933.
18. S. Heidari, N. Masoumi, J. R. Mohassel, N. Karimian, S. Safavi-Naeini, "Analysis and design of defected ground structure for EMC improvement in mixed-signal transceiver modules," IET Science, Measurement & Technology, vol.14, no.7, pp.825-834, Sep. 2020, DOI:10.1049/ietmts.2019.0463.